What is claimed is:

1. An optical coupling arrangement for providing a signal path into and out of a silicon optical waveguide formed in a surface layer of a silicon-on-insulator (SOI) wafer, the optical coupling arrangement comprising

a silicon-based prism coupler permanently attached to the SOI wafer in a manner such that a first, base surface of said prism coupler is disposed substantially parallel to, and mated with, an upper waveguide surface of said SOI wafer, the refractive index of said silicon-based prism coupler at least equal to the refractive index of said silicon optical waveguide; and

an evanescent coupling region disposed between said silicon-based prism coupler and said silicon optical waveguide.

2. An optical coupling arrangement as defined in claim 1 wherein the thickness of the silicon optical waveguide is less than 1 μm.

3. An optical coupling arrangement as defined in claim 1 wherein the silicon optical waveguide is configured to support propagation of a single mode optical signal.

4. An optical coupling arrangement as defined in claim 1 wherein the silicon optical waveguide comprises a multi-layer structure of silicon-based layers, separated by relatively thin dielectric layers.

5. An optical coupling arrangement as defined in claim 1 wherein a second, opposing surface of the silicon-based prism coupler is covered by an anti-reflective (AR) coating.

6. An optical coupling arrangement as defined in claim 1 wherein the species and concentrations of dopants included within the silicon-based prism coupler and the silicon optical waveguide are specified such that the refractive index of said silicon-based prism coupler is equal to or slightly greater than the refractive index of said silicon optical waveguide.

7. An optical coupling arrangement as defined in claim 1 wherein the evanescent coupling region comprises a thin film layer of a material comprising a refractive index less than the refractive index of both the silicon-based prism coupler and the silicon optical waveguide.

8. An optical coupling arrangement as defined in claim 7 wherein the thin film layer evanescent coupling region is formed as a surface layer across the first, base surface of the silicon-based prism coupler.

9. An optical coupling arrangement as defined in claim 7 wherein the thin film layer evanescent coupling region is formed as a surface layer above the silicon optical waveguide layer within the SOI wafer.

10. An optical coupling arrangement as defined in claim 7 wherein the thin film evanescent coupling region comprises a multi-layer structure.

11. An optical coupling arrangement as defined in claim 10 wherein the multi-layer evanescent coupling region comprises at least one layer formed across the first, base surface of the silicon-based prism coupler and at least one layer formed as a surface layer of the SOI wafer.

12. An optical coupling arrangement as defined in claim 7 wherein the evanescent coupling region comprises a thin film of a material chosen from the group consisting of: silicon dioxide, silicon nitride, silicon oxynitride and silicon carbide.

13. An optical coupling arrangement as defined in claim 1 wherein the evanescent coupling region comprises a layer of relatively constant thickness.

14. An optical coupling arrangement as defined in claim 1 wherein the silicon-based prism coupler includes a cavity formed within the first, base surface

15. An optical coupling arrangement as defined in claim 14 wherein the cavity comprises corner edges that sharply truncate an optical beam after a substantial portion of the incident light intensity has been transferred from said silicon-based prism coupler to the silicon optical waveguide.

16. An optical coupling arrangement as defined in claim 14 wherein the cavity is formed using an etching process to form abrupt corner edges along the region where the cavity meets the flat bottom base surface.

17. An optical coupling arrangement as defined in claim 16 wherein an RIE etching process is used to form a cavity with essentially vertical sidewalls.

18. An optical coupling arrangement as defined in claim 16 wherein an anisotropic wet chemical etching process is used to form a cavity with angled sidewalls.

19. An optical coupling arrangement as defined in claim 1 wherein the evanescent coupling region comprises a layer of tapered thickness so as to exhibit a predetermined small thickness in regions where only a small portion of incident light intensity is required to be transferred from the silicon-based prism coupler to the silicon optical waveguide, said thickness thereafter monotonically increasing as the fraction of light intensity transferred from said silicon-based prism coupler to said silicon optical waveguide increases.

20. An optical coupling arrangement as defined in claim 1 wherein the silicon-based prism coupler comprises a single trapezoidal geometry, a first facet of said coupler defined as an input coupler and a second, opposing facet defined as an output coupler, wherein the trapezoidal flat bottom surface is defined as the first, base surface of said prism coupler, said flat bottom surface disposed substantially parallel to the associated SOI wafer.

21. An optical coupling arrangement as defined in claim 20 wherein at least one cavity is formed within the flat bottom base surface of the trapezoidal prism coupler structure.

22. An optical coupling arrangement as defined in claim 21 wherein the surfaces of the cavity are coated with a material having a refractive index that is sufficiently low so as to permit total internal reflection at the corner edges.

23. An optical coupling arrangement as defined in claim 1 wherein the silicon-based prism coupler comprises a pair of trapezoidal prisms, a first trapezoidal prism defined as an input prism and including an input facet for use as an input coupler, and a second trapezoidal prism defined as an output prism and including an output facet for use as an output coupler, the pair of trapezoidal prisms sharing a first, base surface disposed substantially parallel to the SOI wafer.

24. An optical coupling arrangement as defined in claim 1 wherein the silicon-based prism coupler is permanently attached to the SOI wafer by bonding the first, base surface of said silicon-based prism coupler to an upper waveguide surface of said SOI wafer.

25. A method of making a silicon-based prism coupler for use in an arrangement comprising an SOI-based optical device including a silicon optical waveguide layer and

an evanescent coupling layer disposed between the prism coupler and the waveguide, the prism coupler including both input and output ports, the method comprising the steps of:

a) providing a silicon wafer with a refractive index at least equal to the refractive index of the silicon optical waveguide formed in an associated SOI wafer;

b) patterning a first surface of said silicon wafer to define cavity regions;

c) etching said patterned first surface to form cavity regions;

d) patterning a second, opposing surface of said silicon wafer to define facet surfaces for coupling light into and out of the silicon-based prism;

e) anisotropically wet chemical etching the second, opposing patterned surface of said silicon wafer to form V-groove prism facets for input and output coupling; and

f) permanently attaching the etched prism structure of step c) to the associated SOI wafer such that mating surfaces are in optical contact.

26. The method as defined in claim 25 wherein in performing step a), the silicon wafer is oriented along the <100> crystal plane.

27. The method as defined in claim 25 wherein in performing steps b) and c) edges of the cavity region are patterned and etched to define optical coupling regions.

28. The method as defined in claim 25 wherein in performing steps b) and c) the cavity region is formed to include mating surfaces used for the attaching in step f).

29. The method as defined in claim 25 wherein in performing step c) a reactive ion etch process is used.

30. The method as defined in claim 25 wherein in performing step c) an anisotropic wet chemical etch process is used.

31. The method as defined in claim 25 wherein subsequent to performing step e), an isotropic etch process is performed to improve surface flatness.

32. The method as defined in claim 25 wherein in performing step e), the etch process is used to form openings through the complete thickness of the wafer.

33. The method as defined in claim 25 wherein the process further includes the step of depositing an anti-reflective coating over the second surface subsequent to the etching process of step e).

34. The method as defined in claim 33 wherein the anti-reflective coating comprises a single layer of material.

35. The method as defined in claim 34 wherein the material is silicon nitride.

36. The method as defined in claim 33 wherein a multi-layering process is used.

37. The method as defined in claim 25 wherein an evanescent coupling layer is formed over a surface of the associated SOI wafer prior to performing the attachment process of step f).

38. The method as defined in claim 25 wherein a first evanescent coupling layer is formed over at least portions the first surface of the patterned prism wafer and a second evanescent coupling layer is formed over at least portions of the SOI wafer prior to performing the attachment process of step f).

39. The method as defined in claim 25 wherein an evanescent coupling layer is formed over a patterned prism wafer surface prior to performing the attachment process of step f).

40. The method as defined in claim 25 wherein in performing step f), a wafer-to-wafer bonding process is used.

41. The method as defined in claim 25 wherein in performing step f), a die-to-wafer bonding process is used.

42. The method as defined in claim 25 wherein in performing step f), a die-to-die bonding process is used.

43. The method as defined in claim 25 wherein in performing step f) a low temperature bonding process compatible with integrated circuit metallizations systems is used.

44. The method as defined in claim 25 wherein in performing step f) an adhesive material is used.

45. The method as defined in claim 25 wherein in performing step f) a solder-based attachment process is used.

46. The method as defined in claim 25 wherein in performing step f) a process that minimizes electrostatic discharge is used.

47. The method as defined in claim 25 wherein in performing step f) the optically contacted mating surfaces of the SOI wafer are waveguide surfaces located within recessed cavity structures.

48. The method as defined in claim 25 wherein in performing step f), alignment features on the etched prism structure and the associated SOI wafer are used to precisely register the etched prism structure with respect to structures in the SOI wafer.